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Claims

[c1] 1. A method of forming an interconnect structure comprising the steps of:
providing a lower metal wiring layer having first metal lines located within a lower low-k dielectric;
depositing an upper low-k dielectric atop said lower metal wiring layer;
etching at least one portion of said upper low-k dielectric to provide at least one via to said first metal lines;
forming rigid dielectric sidewall spacers in said at least one via of said upper low-k dielectric; and
forming second metal lines in said at least one portion of said upper low-k dielectric.

[c2] 2. The method of Claim 1 wherein said upper low-k dielectric and said lower low-k dielectric comprise materials having a dielectric constant ranging from about 1.0 to about 3.5.

[c3] 3. The method of Claim 1 wherein said upper low-k dielectric and said lower low-k dielectric comprise low-k polymers or low-k carbon doped oxides.

[c4] 4. The method of Claim 1 wherein said rigid dielectric

sidewall spacers comprise SiCH, SiC, SiNH, SiN, or SiO_2.

[c5] 5. The method of Claim 4 wherein said forming rigid dielectric sidewall spacers further comprises:
depositing a conformal rigid dielectric liner atop said upper low-k dielectric and within said at least one via; and
etching horizontal surfaces of said conformal rigid dielectric liner to form said rigid dielectric spacers positioned on vertical sidewalls of said at least one via.

[c6] 6. The method of Claim 5 wherein depositing a conformal rigid dielectric liner further comprises physical vapor deposition (PVD), plasma enhanced chemical vapor deposition (PECVD), high density plasma chemical vapor deposition (HDPCVD), or low pressure chemical vapor deposition (LPCVD).

[c7] 7. The method of Claim 6 wherein said conformal rigid dielectric liner has a thickness ranging from about 10 nm to about 100 nm.

[c8] 8. The method of Claim 7 wherein said etching horizontal surfaces of said conformal rigid dielectric liner further comprises an anisotropic etch process.

[c9] 9. The method 8 wherein said lower metal wiring layer further comprises a rigid insulating layer deposited atop

said lower low-k dielectric, said rigid insulating layer material selected from the group consisting of SiC, SiO_2, and Si_3N_4.

[c10] 10. A method of forming an interconnect structure comprising the steps of:
providing a lower metal wiring layer having first metal lines positioned within a lower low-k dielectric;
depositing a mechanically rigid dielectric atop said lower metal wiring layer;
forming at least one via through said mechanically rigid dielectric to a portion of said first metal lines; and
forming an upper metal wiring layer having second metal lines positioned within a upper low-k dielectric, said second metal lines being electrically connected to said first metal lines through said via, wherein said via comprises a metal having a coefficient of thermal expansion that substantially matches said mechanically rigid dielectric.

[c11] 11. The method of Claim 10 wherein said mechanically rigid dielectric comprises a coefficient of thermal expansion ranging from about 0.1 ppm/^{o}C to about 5.0 ppm/^{o}C.

[c12] 12. The method of Claim 10 wherein said mechanically rigid dielectric comprises SiO_2, SiCOH, or doped silicate

glass.

[c13] 13. The method of Claim 10 wherein said mechanically rigid dielectric has a thickness ranging from about 100 nm to about 1000 nm.

[c14] 14. The method of Claim 10 wherein said upper low-k dielectric and said lower low-k dielectric comprise materials having a dielectric constant of less than about 3.5.

[c15] 15. The method of Claim 14 wherein said upper low-k dielectric and said lower low-k dielectric comprise low-k polymers or low-k carbon doped oxides.

[c16] 16. The method of Claim 15 wherein said low-k polymer is a b-staged polymer comprising about 95% carbon.

[c17] 17. The method of Claim 15 wherein said low-k carbon doped oxide is SiCOH.

[c18] 18. The method of Claim 10 wherein said second metal lines, said first metal lines or a combination of said second metal lines and said first metal lines comprise copper, aluminum, silver, gold or alloys thereof.

[c19] 19. An interconnect structure comprising:
a lower metal wiring level comprising first metal lines positioned within a lower low-k dielectric;
an upper metal wiring level atop said lower metal wiring

level, said upper metal wiring level comprising second metal lines positioned within an upper low-k dielectric; and a plurality of vias through a portion of said upper low-k dielectric electrically connecting said lower metal wiring level and said upper metal wiring level, where said plurality of vias comprise a set of rigid dielectric sidewall spacers.

[c20] 20. The interconnect structure of Claim 19 wherein said set of rigid dielectric sidewall spacers comprise SiCH, SiC, SiNH, SiN, or SiO_2.

[c21] 21. The interconnect structure of Claim 20 wherein each of said set of rigid dielectric sidewall spacers have a thickness ranging from about 10 nm to about 100 nm.

[c22] 22. An interconnect structure comprising:
a lower metal wiring level comprising first metal lines positioned within a lower low-k dielectric;
a mechanically rigid dielectric positioned on said lower metal wiring level, said mechanically rigid dielectric comprising a plurality of metal vias; and
an upper metal wiring level atop said mechanically rigid dielectric, said upper metal wiring level comprising second metal lines positioned within an upper low-k dielectric, where said plurality of metal vias electrically connect said lower metal wiring level and said upper metal wiring

level.

[c23] 23. The interconnect structure of Claim 22 wherein said mechanically rigid dielectric comprises SiO_2, SiCOH, or doped silicate glass.

[c24] 24. The interconnect structure of Claim 22 wherein said plurality of metal vias has a coefficient of thermal expansion matched to said mechanically rigid dielectric.